§112 Rejection of the Claims

Claims 1-45 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The rejection states:

> Claims 1-5, 10-12, 17, 23, 25, 29, 32, 33, 37-40, 44 and 45 are misdescriptive and renders the claims indefinite as reciting the pair of transistors M3, M5 and M4, M6 is a dual-gated transistor. It is well known in the art that a dual-gated transistor is an AND function circuit. However, the pair of transistors M3, M5 and M4, M6 are the OR function circuit. Therefore, the pair of transistors M3, M5 and M4, M6 can not be replaced with a dual-gated transistor. Claims 6-9, 13-17, 18-22, 24, 26-28, 30-31, and 41-43 are rejected as including the indefiniteness of one of the claims above.

The Examiner correctly notes that the pair of "dual-gated" transistors M3, M5 and M4, M6 of the present invention are the OR function circuit. The Examiner misrepresents, however, that **all** dual gate transistors must be an AND function circuit. This is **only** the case for conventional MESFET transistors, which have a pair of gates located only on one side of a single body region of a transistor. The conventional dual-gate MESFET is **not** referenced or described in the Applicant's case.

In contrast, the Applicant's specification (at page 10), drawings, and claims all reference a "dual-gated" transistor having a pair of gates on opposing sides of a single body region for a transistor. Applicant's "dual-gated transistor structure represents another configuration for dual gate transistors. In this configuration two separate n-channel regions are formed in the single body region on opposing sides of the body region by independent potentials applied to the dual gates. Such a configuration is also referred to as a dual-gate or double-gated structure in silicon technology and performs the OR function. Therefore, Applicant's pair of transistors M3, M5 and M4, M6 are indeed "dual-gated" transistors. One of ordinary skill in the art will know and understand the same upon reading the Applicant's disclosure. This structure can be further understood by reference to US patent number 6,104,068 which shares a common inventor to the

present case. In view of these remarks, reconsideration and withdrawal of the 112 rejection for the above listed claims is respectfully requested.

§102 Rejection of the Claims

Claims 1-7, 10-14, 17-20, 29, 32-39, 44 and 45 were rejected under 35 USC § 102(b) as being anticipated by Kawashima (U.S.5,699,305). The rejection states:

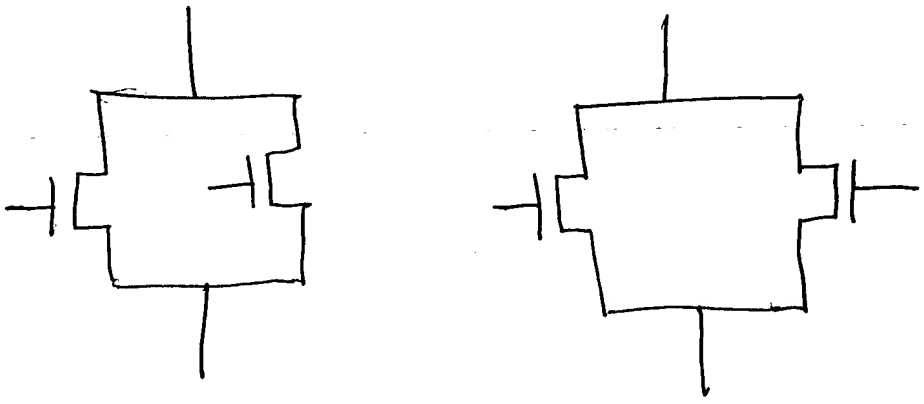
> Kawashima discloses in figure 7 a sense amplifier (105) comprising: a pair of cross-coupled inverters (66-69, and 72-75), wherein each inverter includes: a transistor of a first conductivity type (66, 67), a dual gated transistor of second conductivity type (68, 69, 74, 75) wherein a drain region for the dual-gated transistor is coupled to a drain region of the transistor of the first conductivity type; a pair of bit lines (IN, /IN), wherein each one of the pair of bit lines is coupled to a first gate of the dual-gated transistor in each inverter; and a pari of bit lines is coupled to a first gate of the dual-gated transistor in each inverter; and a pair of output transmission lines (OUT, /OUT), wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gated transistor and the drain region of the transistor of the first conductivity type in each inverter.

Kawashima appears to describe an amplifier and semiconductor memory device having the same. The amplifier is coupled to first and second power supply lines. Kawashima further describes a first pair of cross-coupled transistors connected to the first power supply line and a pair of output terminal, and a second pair of cross-coupled transistors connected to the second power supply line. The amplifier includes a pair of **input transistors** (e.g. 74 and 75, which are separate transistor structures altogether and do not share a single body region) connected to the second pair of cross-coupled transistors. (See Abstract). Kawashima does **not** describe **a dual gated transistor of a second conductivity type** as pointed to by the examiner at 68, 69, 74, and 75. Rather, the transistors referenced by the examiner include **four** independent transistor device structures coupled in parallel.

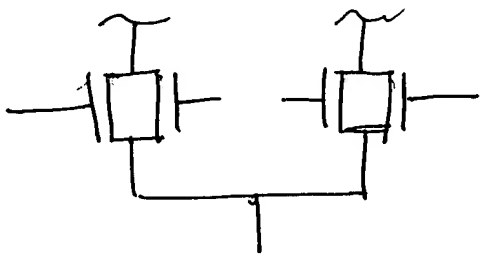
In contrast, each of the Applicant's independent claims recite a "dual gate transistor" as a positive limitation to the Applicant's invention. As used in the Applicant's specification, a "dual gate transistor" includes a transistor in which a single body region is driven on opposing sides by

two separate gates. This facilitates the high performance, wide bandwidth, or very fast CMOS amplifier of the present invention which is as much as 100 times faster than conventional voltage sense amplifiers when low power voltage supplies of less than 1.0 Volts are utilized. The same is explained in more detail in connection with Figure 2C. As outlined in the Applicant's specification on page 10, lines 16-30, the pair of transistors, (the first being M3, M5 and the second being M4, M6) in each inverter, B1 and B2, comprise a **dual gated** metal oxide semiconductor field effect transistor (MOSFET). One of the pair of transmission lines is coupled to a first gate of the dual-gated MOSFET in each inverter, B1 and B2. The transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and the dual gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors, each driven by one of the dual gates. The drain regions, 204 and 212, for one of the cross-coupled inverters, B1, is further coupled to a gate of the transistor of the first conductivity type, M2, and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters, B1 and B2. Similarly, the drain regions, 206 and 214, for inverter, B2, is coupled to a gate of the transistor of the first conductivity type, M1, and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters, B1 and B2.

This means, in effect, that two separate n-channel regions are formed in the single body region on opposing sides of the body region by independent potentials applied to the dual gates, and not that there are two physically separate transistors. Kawashima illustrates in the representation of transistors 68, 69, 74, and 75, a set of conventional separate NMOSFETs connected in parallel. The sketches below illustrate the same.



There is no conventional circuit symbol for a "dual-gated" or "double-gated" MOSFET of the type used and claimed in the Applicant's invention. However, Applicant's Figure 2A and Figure 3 serve to best represent a single transistor body driven by two gates. This representation is reproduced for the Examiner's convenience below.



The sketch above represents either dual gated transistor (M3, M5) or dual gated transistor (M4, M6). The "box-like" structure with gates on both sides is clearly meant to designate a dual-gated or double-gated NMOSFET having a singly body region, and not simply two separate MOSFETS which would be more typically represented by the earlier sketches above. This structure can be further understood by reference to US patent number 6,104,068 which shares a common inventor to the present case. The terms "dual-gate" or "double-gate" are both commonly used in silicon technology for gates on opposing sides of a single body region and distinguish from reference to transistors simply connected in parallel as shown in Kawashima. This description of a dual-gate transistor is further to be distinguished from denoting a "dual-gate" MESFET transistor which have gates in series on only one side of a single transistor body region and which are used with microwave devices to perform an AND function circuit.

In sum, Kawashima does not teach or suggest a "dual-gated" transistor as described herein in connection with the Applicant's specification, drawings, and as claimed in each of the Applicant's independent claims. Thus, the Kawashima reference does not include each and every limitation of the Applicant's independent claims. Accordingly reconsideration and withdrawal of the 102 rejection for each of the Applicant's independent claims, as well as those claims which depend therefrom, is respectfully requested.

§103 Rejection of the Claims

Claims 8, 9, 15-22, 30 and 31 were rejected under 35 USC § 103(a) as being unpatentable over Kawashima (U.S. 5,699,305). For the reasons presented above, Applicant believes that each of the present independent claims as well as those claims which depend therefrom are distinguishable from the Kawashima reference. In view of those remarks, reconsideration and withdrawal of the 103 rejections for the above listed claims is respectfully requested.

Claims 23-28 and 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al. (U.S. 6,069,828) in view of Kawashima (U.S. 5,699,305). Again, Kawashima does not teach or suggest each and every limitation of the Applicant's claims cited above. Specifically, Kawashima does not teach or suggest the use of a "dual-gated" transistor as defined in the Applicant's novel circuit configuration for improved sense amplifiers. Additionally the Kaneko reference does not teach or suggest "dual-gated" transistors, as described herein, and thus does not cure the deficiencies of the Kawashima reference. Since neither the Kawashima or Kaneko reference, either independently or in combination, teach each and every element and limitation of the above cited claims, reconsideration and withdrawal of the rejection for the same is respectfully solicited.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at 612-373-6913 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date 2/8/2001 By

Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 8th day of February, 2001.

Amy Moriarty
Name

Amy Moriarty
Signature